Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-42 (Canceled)

43. (Currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a first dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and ~~over~~ said first dielectric layer, wherein a first opening in said passivation layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, ~~and~~ wherein a second opening in said passivation layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a third opening in said passivation layer is over a third contact point of a third metal interconnect of said metallization structure, and said third contact point is at a bottom of said third opening, ~~wherein a gap is between said first and second metal interconnects,~~ wherein said first contact point is connected to said third contact point through said resistor, wherein said passivation layer comprises ~~an insulating~~ a nitride layer; and

a third metal layer ~~circuit trace~~ over said passivation layer and on said first, ~~and~~ second and third contact points, wherein said first contact point is connected to said second contact point through a first portion of said third metal layer, wherein said third metal layer comprises a second portion connected to said first portion of said third metal layer through, in sequence, said third contact point, said resistor and said first contact point. ~~said circuit trace.~~

44. (Previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises boron.

45. (Previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises phosphorous.

46. (Previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises arsenic.

47. (Previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises gallium.

48. (Currently amended) The chip structure as claimed in claim 43 further comprising a polymer layer on said passivation layer, wherein said third metal layer ~~circuit trace~~ is further on said polymer layer.

49. (Previously presented) The chip structure as claimed in claim 48, wherein said polymer layer comprises polyimide (PI).

50. (Previously presented) The chip structure as claimed in claim 48, wherein said polymer layer comprises benzocyclobutene (BCB).

51. (Currently amended) The chip structure as claimed in claim 43 further comprising a polymer layer on said third metal layer ~~circuit trace~~ and over said passivation layer.

52. (Previously presented) The chip structure as claimed in claim 51, wherein said polymer layer comprises polyimide (PI).

53. (Previously presented) The chip structure as claimed in claim 51, wherein said polymer layer comprises benzocyclobutene (BCB).

54. (Currently amended) The chip structure as claimed in claim 43 further comprising an inductor over said silicon substrate, wherein said inductor comprises a portion provided by said third metal layer. ~~passivation layer.~~

55. (Currently amended) The chip structure as claimed in claim 54, wherein said third metal layer ~~inductor~~ comprises a copper layer.

56. (Currently amended) The chip structure as claimed in claim 54, wherein said third metal layer ~~inductor~~ comprises a gold layer.

57. (Currently amended) The chip structure as claimed in claim 54, wherein said third metal layer ~~inductor~~ comprises a titanium-containing layer and a copper layer over said titanium-containing layer.

58. (Canceled)

59. (Currently amended) The chip structure as claimed in claim 43 further comprising a capacitor over said silicon substrate, wherein said capacitor comprises a first electrode, provided by said metallization structure, over said silicon substrate, wherein a ~~third~~ fourth opening in said passivation layer is over said first electrode, a second dielectric layer on said first electrode and in said ~~third~~ fourth opening, and a second electrode, provided by said third metal layer, on said second dielectric layer and over said first electrode.

60. (Canceled)

61. (Currently amended) The chip structure as claimed in claim 43, ~~60,~~ wherein said third metal layer ~~second electrode further~~ comprises a titanium-containing layer and ~~under said~~ a gold layer over said titanium-containing layer.

62. (Canceled)

63. (Currently amended) The chip structure as claimed in claim 59, wherein said third metal layer ~~second electrode~~ comprises a copper layer and a nickel layer over said copper layer.

64. (Currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a ~~passivation~~ nitride layer over said metallization structure and ~~over~~ said dielectric layer, wherein a first opening in said ~~passivation~~ nitride layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said ~~passivation~~ nitride layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, ~~wherein a gap is between said first and second metal interconnects,~~ wherein said first contact point is connected to said second contact point through said resistor, wherein said ~~passivation~~ nitride layer has a thickness greater than 0.35 micrometers; ~~comprises an insulating nitride layer;~~ and

a third metal layer ~~circuit trace~~ over said nitride ~~passivation~~ layer and on said first and second contact points, wherein said third metal layer comprises a first portion connected to a second portion of said third metal layer through, in sequence, said first contact point, said resistor and said second contact point, ~~first contact point is connected to said second contact point through said circuit trace,~~ wherein said ~~circuit trace~~ third metal layer comprises a copper ~~titanium containing~~ layer. ~~and a gold layer over said titanium containing layer.~~

65. (Previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises boron.

66. (Previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises phosphorous.

67. (Previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises arsenic.

68. (Previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises gallium.

69. (Currently amended) The chip structure as claimed in claim 64 further comprising a polymer layer on said ~~passivation~~ nitride layer, wherein said third metal layer ~~circuit trace~~ is further on said polymer layer.

70. (Previously presented) The chip structure as claimed in claim 69, wherein said polymer layer comprises polyimide (PI).

71. (Previously presented) The chip structure as claimed in claim 69, wherein said polymer layer comprises benzocyclobutene (BCB).

72. (Currently amended) The chip structure as claimed in claim 64 further comprising a polymer layer on said third metal layer ~~circuit trace~~ and over said ~~passivation~~ nitride layer.

73. (Previously presented) The chip structure as claimed in claim 72, wherein said polymer layer comprises polyimide (PI).

74. (Previously presented) The chip structure as claimed in claim 72, wherein said polymer layer comprises benzocyclobutene (BCB).

Claims 75-82 (Canceled)

83. (Currently amended) The chip structure as claimed in claim 64, wherein said third metal layer further comprises a titanium-containing layer under said copper layer. ~~comprises a titanium-tungsten alloy.~~

84. (Currently amended) The chip structure as claimed in claim 64, wherein said nitride layer comprises silicon nitride. ~~metallization structure comprises aluminum.~~

Claims 85-88 (Canceled)

89. (Currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a separating ~~passivation~~ layer over said metallization structure and ~~over~~ said dielectric layer, wherein a first opening in said separating ~~passivation~~ layer is over a first contact point of a first metal interconnect of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said separating ~~passivation~~ layer is over a second contact point of a second metal interconnect of said metallization structure, and said second contact point is at a bottom of said second opening, ~~wherein a gap is between said first and second metal interconnects,~~ wherein said first contact point is connected to said second contact point through said resistor, wherein said separating ~~passivation~~ layer comprises ~~an insulating~~ a nitride layer; ~~and~~

a third metal layer ~~circuit trace~~ over said separating ~~passivation~~ layer and on said first and second contact points, wherein said third metal layer comprises a first portion connected to a second portion of said third metal layer through, in sequence, said first contact point, said resistor and said second contact point, ~~first contact point is connected to said second contact point through said circuit trace,~~ wherein said third metal layer ~~circuit trace~~ comprises a copper layer; and ~~.~~

a first polymer layer covering a top surface and sidewall of said first portion of said third metal layer.

90. (Previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises boron.

91. (Previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises phosphorous.

92. (Previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises arsenic.

93. (Previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises gallium.

94. (Currently amended) The chip structure as claimed in claim 89 further comprising a second polymer layer on said ~~passivation~~ separating layer, wherein said ~~circuit trace~~ third metal layer is further on said second polymer layer.

95. (Currently amended) The chip structure as claimed in claim 94, wherein said second polymer layer comprises polyimide (PI).

96. (Currently amended) The chip structure as claimed in claim 94, wherein said second polymer layer comprises benzocyclobutene (BCB).

97. (Currently amended) The chip structure as claimed in claim 89, wherein said third metal layer further comprises a titanium-containing layer under said copper layer. ~~further comprising a polymer layer on said circuit trace and over said passivation layer.~~

98. (Currently amended) The chip structure as claimed in claim 89, ~~97,~~ wherein said first polymer layer comprises polyimide (PI).

99. (Currently amended) The chip structure as claimed in claim 89, ~~97,~~ wherein said first polymer layer comprises benzocyclobutene (BCB).

100. (Currently amended) The chip structure as claimed in claim 89, wherein said ~~circuit trace~~ third metal layer further comprises a nickel layer over said copper layer.

101. (Currently amended) The chip structure as claimed in claim 89, wherein said third metal layer ~~circuit trace~~ further comprises a gold layer over said copper layer.

102. (Currently amended) The chip structure as claimed in claim 89, wherein said third metal layer ~~circuit trace~~ further comprises a nickel layer over said copper layer, and a gold layer over said nickel layer.